AMENDMENTS TO THE CLAIMS:

Please replace the last paragraph on page 20 (ending on page 21) with the following:

Fig. 20 is a refined top plan layout 1200 illustrating a single exemplary eDRAM memory cell 1205 ~~1005~~, according to a fourth aspect of the present invention, wherein a modified contact pattern provides a contact pillar used in the storage plate connected to the active region. In this view of the eDRAM cell 1205 ~~1005~~, a modified contact pillar provides a storage plate 1225 with features which produce added surface area for greater capacitance. The storage plate is also connected to the storage node of the active region 214, and is formed within the confines of a larger capacitor ground plate 1276 within the capacitor region 210. Fig. 20 also shows that the capacitor region 210, forms one wall of the trench as an etching boundary within the PMD layer 265, while the other three walls of the trench, are defined by the surrounding walls of the contact structure forming the ground plate 1276. As in the third aspect of the present invention, the left edge of the modified contact pillar remains partially embedded within the PMD for added structural integrity during processing.

Please replace the second full paragraph on page 21 with the following:

Again, in accordance with the fourth aspect of the present invention, a three dimensional capacitor is formed in a trench etched, for example, about 0.4 microns deep within the PMD layer 265. A large capacitor ground plate 1276 ~~1045~~, a capacitor dielectric layer 270, and the smaller generally rectangular

storage plate 1225, are formed in a trench within the PMD layer 265. The ground plate 1276 of the capacitor is formed as a generally continuous structure along an axis of the ground plane, with latterly extending portions anchored into the PMD material. This layout yields structural support and increased capacitor surface area. An STI region 260 isolates the active areas 214. The bit line contact 218 is formed along with the ground plate contact structure (not shown) by the M1 metal layer deposition of conductive material through openings formed in the M1 dielectric layer 280.